Manu Awasthi

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Web www.manuawasthi.in

Research Interests

Computer architecture and systems, memory and storage systems, performance characterization and modeling, computers and society

Education

Ph.D., Computer Science 2005 - 2011
University of Utah, Salt Lake City, UT
Advisor - *Prof. Rajeev Balasubramonian*

B. Tech, Computer Science and Engineering 2001 - 2005
Institute of Technology, Banaras Hindu University (BHU), Varanasi, IN

Awards and Fellowships

- Research Excellence Fellowship, IIT Gandhinagar, 2016 - 2018
- Best Paper Award, ICPE 2015
- Second prize, Micron ADG ideas brainstorming, November 2012
- Best Paper Award, PACT 2010
- School of Computing, University of Utah Teaching Fellowship, 2005 - 2006

Research Grants

- Huawei India, Unrestricted Research Grant INR 26,00,000 (2021-2022)
- Lam Research, Unrestricted Research Grant USD 8,000 (2020)
- Semiconductor Research Corporation, USD 13,500 (2020-2023)
- Ashoka University Startup Grant, INR 15,00,000 (2019-2021)
- Ashoka University grant to organize Workshop on Computer Systems, INR 2,00,000 (2018)
- Early Career Research Award (ECRA) from Science and Education Research Board (SERB), INR 26,24,600 (2017 - 2020)
- IIT Gandhinagar grant to organize Workshop on Computer Systems 2017, INR 50,000 (2017)
- IIT Gandhinagar Research Grant, INR 30,00,000 (2017 - 2020)
- Research Excellence Fellowship, IIT Gandhinagar (2016 - 2018)

Experience

Visiting Researcher, Amuse Labs
May 2020 - April 2021 , Bangalore, India

Associate Professor, Computer Science, Ashoka University
August 2018 - Present , Sonipat, Haryana, India

Assistant Professor, Indian Institute of Technology, Gandhinagar
November 2016 - August 2018, Gandhinagar, Gujarat, India

- Teaching and research in computer systems
- Teaching graduate and undergraduate courses in Computer Architecture, Operating Systems and Programming Languages.

System Architect : Memory Solutions Lab, *Samsung Semiconductor*
December 2013 - September 2016, San Jose, CA

- Design and performance evaluation of memory and storage architectures for large scale computer systems including datacenter/big-data applications and use cases.
- Responsibilities include full-system characterization and analysis of datacenter workloads from hardware to the application through the operating system stack to locate performance bottlenecks;utilize learnings to drive next generation storage architectures.
- Developed reference designs for next generation Big Data storage solutions; work showcased at Flash Memory Summit, 2015
- Collaborating with universities for research in datacenter storage systems.

Architect : Architecture Development Group, *Micron Semiconductor*
October 2011 - December 2013, Boise, ID

- Design and performance evaluation of DRAM architectures including LPDDR, DDR3, DDR4, and 3/2.5 D architectures.
- Responsibilities included development of modeling and simulation infrastructure for performance and power characteristics of DRAM architectures; integrating these models with full-system architectural simulators. Part of a two person team that ported gem5 to SystemC.
- Projects included evaluating novel multi-channel DRAM (DDR3, DDR4, 2.5D) architectures and addressing mechanisms.
- Consulted with Micron Ventures to evaluate new memory architectures, technologies and IP for technical feasibility.

Peer-Reviewed Publications [1]

1. **ANSim: A Fast and Versatile Asynchronous Network-On-Chip Simulator**, Tom Glint, Jitesh Sah, Manu Awasthi and Joycee Mekie, *38th IEEE International Conference on Computer Design*, **ICCD**, October 2020

2. **Prefetching in Hybrid Main Memory Systems**, Subisha V, Varun Gohil, Nisarg Ujjainkar, *Manu Awasthi*, *12th USENIX Workshop on Hot Topics in Storage and File Systems*, **HotStorage**, July 2020

3. **Exploring Trends in Higher Education in India**, Saloni Bhogale, *Manu Awasthi*, *Indian Public Policy Network Annual Conference*, March 2020

4. **Efficacy of Statistical Sampling on Contemporary Workloads: The Case of SPEC CPU2017**, Sarabjeet Singh, *Manu Awasthi*, *IEEE International Symposium on Workload Characterization*, **IISWC**, November 2019

[1] 1409 Total Citations, h-index 16, January, 2021, per Google Scholar

5. **FAB: Framework for Analyzing Benchmarks**, Varun Gohil, Shreyas Singh, *Manu Awasthi*, *International Conference on Performance Engineering*, **ICPE**, *Work in Progress track*, April 2019

6. **Memory Centric Characterization and Analysis of SPEC CPU2017 Suite**, Sarabjeet Singh, *Manu Awasthi*, *International Conference on Performance Engineering*, **ICPE**, April 2019

7. **META: Memory Exploration Tool for Android Devices**, Nisarg Parikh, Varun Gohil, *Manu Awasthi*, *International Conference on Mobile Computing and Networking*, **MobiCom**, October 2018 **(Poster)**

8. **I/O Workload Management for All-Flash Datacenter Storage Systems Based on Total Cost of Ownership**, Zhengyu Yang, *Manu Awasthi*, Mrinmoy Ghosh, Janki Bhimani and Ningfang Mi, *IEEE Transactions on Big Data*, September 2018.

9. **Docker Container Scheduler for I/O Intensive Applications running on NVMe SSDs**, Janki Bhimani, Zhengyu Yang, Ningfang Mi, Jingpei Yang, Qiumin Xu, *Manu Awasthi*, Rajinikanth Pandurangan, Vijay Balakrishnan, *IEEE Transactions on Multi-Scale Computing Systems*, Vol. 4, Issue 3, September 2018

10. **Exploring Non-Volatile Main Memory Architectures for Handheld Devices**, Sneha Ved, *Manu Awasthi*, *IEEE Conference on Design Automation and Test in Europe*, **DATE**, March, 2018

11. **Rack Level Scheduling for Containerized Workloads**, Qiumin Xu, Krishna T. Malladi, *Manu Awasthi International Conference on Networking, Architecture, and Storage*, **NAS**, August, 2017 **(Poster)**

12. **Performance Analysis of Containerized Applications on Local and Remote Storage**, Qiumin Xu, *Manu Awasthi*, Krishna T. Malladi, Janki Bhimani, Jingpei Yang, Murali Annavaram, *International Conference on Massive Storage Systems and Technology*, **MSST**, May, 2017

13. **Docker Characterization on High Performance SSDs,** Qiumin Xu, *Manu Awasthi*, Krishna T. Malladi, Janki Bhimani, Jingpei Yang, Murali Annavaram, *International Symposium on Performance Analysis of Systems and Software*, **ISPASS**, April, 2017 **(Poster)**

14. **KOVA : A tool for Kernel Visualization and Analysis** Manu Awasthi, Krishna T. Malladi, *International Performance Computing and Communications Conference*, **IPCCC**, December 2016 **(Poster)**

15. **Understanding Performance of I/O Intensive Containerized Applications for NVMe SSDs** Janki Bhimani, Jingpei Yang, Zhengyu Yang, Ningfang Mi, Qiumin Xu, Manu Awasthi, Rajinikanth Pandurangan, Vijay Balakrishnan, *International Performance Computing and Communications Conference*, **IPCCC**, December 2016

16. **A Fresh Perspective on the Total Cost of Ownership of SSDs** Zhengyu Yang, Manu Awasthi, Mrinmoy Ghosh, Ningfang Mi, *International Conference on Cloud Computing Technology and Science*, **CloudCom**, December 2016

17. **FlexDrive: A Framework to Explore NVMe Storage Solutions** Krishna T. Malladi, Manu Awasthi, Hongzhong Zheng, *International Conferences on High Performance Computing and Communications*, **HPCC**, December, 2016

18. **DRAMScale: Mechanisms to increase DRAM Capacity** Krishna T. Malladi, Manu Awasthi, Hongzhong Zheng, *International Conference on Memory Systems*, **MEMSYS**, October, 2016

19. **DRAMPersist: Making DRAM Systems Persistent** Krishna T. Malladi, Manu Awasthi, Hongzhong Zheng, *International Conference on Memory Systems*, **MEMSYS**, October, 2016

20. **Software-Defined Emulation Infrastructure for High Speed Storage** Krishna T. Malladi, Manu Awasthi, Hongzhong Zheng, *International Systems and Storage Conference*, **SYSTOR**, May, 2016 **(Poster)**

21. **Rethinking Design Metrics for Datacenter DRAM** Manu Awasthi, *International Conference on Memory Systems*, **MEMSYS**, October, 2015

22. **Performance Analysis of NVMe SSDs and their Implication on Real World Databases** Qiumin Xu, Huzefa Siyamwala, Mrinmoy Ghosh, Manu Awasthi, Tameesh Suri, Zvika Guz, Anahita Shayesteh, Vijay Balakrishnan, **SIGMETRICS**, June, 2015 **(Poster)**

23. **Performance Characterization of Hyperscale Applications on NVMe SSDs** Qiumin Xu, Huzefa Siyamwala, Mrinmoy Ghosh, Tameesh Suri, Manu Awasthi, Zvika Guz, Anahita Shayesteh, Vijay Balakrishnan, *International Systems and Storage Conference*, **SYSTOR**, May, 2015

24. **Performance Characterization of Realistic Hyperscale Applications on NVMe SSDs** Qiumin Xu, Manu Awasthi, Tameesh Suri, Zvika Guz, Anahita Shayesteh, Mrinmoy Ghosh, Vijay Balakrishnan, *Annual Non-Volatile Memories Workshop*, **NVMW**, March, 2015 (Poster)

25. **System Level Characterization of Datacenter Applications** Manu Awasthi, Tameesh Suri, Zvika Guz, Anahita Shayesteh, Mrinmoy Ghosh, Vijay Balakrishnan, *International Conference on Performance Engineering*, **ICPE**, February, 2015 (Best Paper Award)

26. **Real-Time Analytics as the Killer Application for Processing-In-Memory** Zvika Guz, Manu Awasthi, Vijay Balakrishnan, Mrinmoy Ghosh, Anahita Shayesteh, Tameesh Suri, *Workshop on Near Data Processing*, **WoNDP**, December, 2014

27. **Performance Analysis of Multi-Channel DDR3 DRAM** Manu Awasthi, David A. Roberts, Robert Walker, J. Thomas Pawlowski, *Micron DRAM Products Technical Seminar*, **DPTS**, September, 2012

28. **Full-system, Memory-Oriented Performance Modeling Tools using Multi-Core CPUs and GPUs** David A. Roberts, Manu Awasthi, Robert Walker, J. Thomas Pawlowski, *Micron DRAM Products Technical Seminar*, **DPTS**, September, 2012

29. **USIMM : the Utah SImulated Memory Module** Niladrish Chatterjee, Rajeev Balasubramonian, Manjunath Shevgoor, Seth Pugsley, Aniruddha Udipi, Ali Shafiee, Manu Awasthi, Kshitij Sudan, Zeshan Chisti, *University of Utah, School of Computing Technical Report TR-UUCS-12-002, Technical Report for JWAC Memory Scheduling Competition*, February 2012

30. **Managing Resistance Drift in Phase Change Memory** Manu Awasthi, Manjunath Shevgoor, Kshitij Sudan, Rajeev Balasubramonian, Bipin Rajendran, Viji Srinivasan, *International Conference on High Performance Computer Architecture*, **HPCA**, February 2012

31. **Predictor-Based Management of DRAM Row-Buffers in the Many-Core Era** Manu Awasthi, David Nellans, Kshitij Sudan, Rajeev Balasubramonian, Al Davis, *International Conference on Parallel Architectures and Compilation Techniques*, **PACT**, September, 2011 (poster track)

32. **Managing Data Placement in Memory Systems with Multiple Memory Controllers** Manu Awasthi, David Nellans, Kshitij Sudan, Rajeev Balasubramonian, Al Davis, *International Journal of Parallel Programming*, **IJPP**, Volume 40, Issue 1, 2011

33. **Handling PCM Resistance Drift with Device, Circuit, Architecture and System Solutions** Manu Awasthi, Manjunath Shevgoor, Kshitij Sudan, Rajeev Balasubramonian, Bipin Rajendran, Viji Srinivasan, *Annual Non-Volatile Memories Workshop*, **NVMW**, March, 2011

34. **Handling the Problems and Opportunities Posed by Multiple On-Chip Memory Controllers** Manu Awasthi, David Nellans, Kshitij Sudan, Rajeev Balasubramonian, Al Davis, *International Conference on Parallel Architectures and Compilation Techniques*, **PACT**, September, 2010 (Best Paper Award)

35. **Increasing DRAM Efficiency with Locality-Aware Data Placement** Kshitij Sudan, Niladrish Chatterjee, David Nellans, Manu Awasthi, Rajeev Balasubramonian, Al Davis, *International Conference on Architectural Support for Programming Languages and Operating Systems*, **ASPLOS**, March, 2010

36. **Dynamic Hardware-Assisted Software Controlled Page Placement to Manage Capacity Allocation and Sharing within Large Caches** Manu Awasthi, Kshitij Sudan, Rajeev Balasubramonian, John Carter, *International Conference on High Performance Computer Architecture*, **HPCA**, February, 2009

37. **Scalable and Reliable Communication for Hardware Transactional Memory** Seth Pugsley, Manu Awasthi, Niti Madan, Naveen Muralimanohar, Rajeev Balasubramonian, *International Conference on Parallel Architecture and Compilation Techniques*, **PACT**, October, 2008

38. **Understanding the Impact of 3D Stacked Layouts on ILP** Manu Awasthi, Vivek Venkatesan, Rajeev Balasubramonian, *Journal of Instruction Level Parallelism*, **JILP**, Volume 9, 2007

39. **Exploring the Design Space for 3D Clustered Architectures** Manu Awasthi,

Rajeev Balasubramonian, *IBM Watson Conference on Interaction between Architecture, Circuits, and Compilers*, **P=ac^2**, October, 2006

Popular Media Articles

1. How the Indian Government Can Help Improve the Ease of Doing Research, The Wire, 30^{th} June, 2020
2. Why I Science When Others Protest, The Wire, 31^{st} December, 2019

Patents and Patent Applications

1. Architecture for achieving high throughput for key-value caching infrastructures, providing better efficiency and TCO, US14/595172 **(Granted)**
2. Data Management Scheme in Virtualized Hyperscale Environments, US14/729026 (Application)
3. Address Translation in Memory, US14/813111 (Application)
4. DRAM aware OS Page Organization, US14/674399 (Application)
5. WAF and TCO Aware Online Flash Resource Allocation Manager, US15/092156 (Application)
6. TCO/WAF Based Online Flash Resource Migration, Allocation, Retirement and Replacement Manager, US15/094971 (Application)
7. Online Stream Filter Assisted, Log Buffer-Based Multiple-Associative Sector Translation FTL Design (SLMAST), US15/093682 (Publication)
8. Multi-bit data representation framework to enable dual program operation on solid-state flash devices, US15/217964 (Application)
9. Block Cleanup: Page reclamation process to reduce garbage collection overhead in dual-programmable NAND Flash devices, US15/405227 (Application)
10. Intelligent controller for Containerized Applications, US15/379327 (Application)
11. I/O Workload Scheduling Manager for RAID/non-RAID Flash based Storage Systems for TCO and WAF optimizations, US15/396186 (Application)
12. Rack-level Scheduling for Reducing the Long Tail Latency using High Performance SSDs, US15/467458 (Application)

Unrefereed Posters

1. **ABP : Predictor Based Management of DRAM Row Buffers**, School of Computing , University of Utah Graduate Research Day, Spring 2010
2. **Controlling Page Placement to Manage Large Caches** (Best Poster Runner-up), School of Computing , University of Utah Graduate Research Day, Spring 2009
3. **Scalable and Reliable Communication for Hardware Transactional Memory**, School of Computing , University of Utah Graduate Research Day, Spring 2008
4. **Understanding the Impact of 3D Stacked layouts on ILP, School of Computing** , University of Utah Graduate Research Day, Spring 2007

Tool Development

1. **ANSim : the Utah SImulated Memory Module** is a fast and versatile Asynchronous Network-on-Chip (NoC) Simulator. ANSim can model routers with different delays, routers with asynchronous arbitration, connected in a wide range of topologies. ANSim supports individual routers modeled to have varying timing constraints and supports synthetic and real-workloads, and produces system-level latency, throughput, power, power-gating, and arbitration reports. The tool can be downloaded here.

2. **USIMM : the Utah SImulated Memory Module** I contributed to the development of USIMM, a trace-based simulation infrastructure for modeling the DRAM sub-system, including timing parameters and memory controller functionalities. The tool can be downloaded here.

Curriculum Development

1. CS 326/ES 215 Computer Architecture: Designed and taught the first course on Computer Architecture at IIT Gandhinagar.

2. CS 612 Computer Systems: Designed and currently teaching the PG course on Computer Systems, which encompasses elements of computer architecture, operating systems and distributed systems for early stage graduate students. The course is formatted to serve as a refresher for the fundamentals taught in undergraduate classes and add a number of hands-on, implementation based assignments to give the students a broad overview of the possibilities in the area.

Teaching

1. Operating Systems, Advanced Computer Architecture : Spring 2019, 2020

2. Computer Organization and Systems, Programming Language Design and Implementation : Monsoon 2018, 2019, 2020

3. Spring 2018 - ES 215 - Computer Organization and Architecture (UG, 46 students)

4. Fall 2017 - CS 612 - Computer Systems (PG, 20 students, student rating **3.66/4**), FP 101 - Foundation Program (173 students)

5. Spring 2017 - CS 326 - Computer Architecture (UG, 27 students, student rating **3.38/4**)

6. Summer 2017, Fall 2017, Spring 2018 Systems Reading Group (Seminar)

Conference and Workshop Organization

1. **CAWS 2020**: Computer Architecture Winter School. December, 2020. Organizer. CAWS was a four day winter school organized to bring together researchers from industry and academia to talk about recent advances in computer systems, including computer architecture, compilers and operating systems.

2. **WoCS 2018**: **W**orkshop on **C**omputer **S**ystems. December, 2018. Organizer. WoCS was a two day workshop organized to bring together researchers from industry and academia to talk about recent advances in computer systems, including computer architecture, compilers, operating systems and programming languages.
3. **ROCS 2017**: **R**esearch **O**pportunities in **C**omputer **S**cience, February, 2017, co-organizer. ROCS was a one day event held at IIT Gandhinagar to introduce undergraduates and early stage graduate students to various research opportunities in computer science and engineering.
4. **WoMS 2017**: **W**orkshop on **M**emory and **S**torage Systems. December, 2017. Organizer. WoMS was a two day workshop organized to bring together researchers from industry and academia to collaborate towards solving the most pressing issues in memory and storage systems.

Outreach

1. Computer Architecture Summer School (CASS 2018): Co-organizer and Instructor
2. High School teacher training - Kendriya Vidyala (KV) Computer Science teachers. Taught computer architecture and audrino related concepts to 55 KV teachers (June 2018).
3. Vigyan Jyoti - Taught computer architecture and audrino related concepts to class 11^{th} girl students under Government of India's Vigyan Jyoti scheme (June 2018)

Mentoring

Current

1. Varun Gohil, Research Fellow, since July 2020.
2. Tom Glint Issac, PhD student, co-supervised with Prof. Joycee Mekie (IITGn), since Fall 2017

Past

1. Sarabjeet Singh, Junior Research Fellow, Jan 2018 - July 2019.
2. Prathamesh Upadhyay, M.Tech student, co-supervised with Prof. Neeldhara Misra (IIT Gandhinagar), graduated August 2020.
3. Subisha V, M.Tech student, graduated July 2019
4. Nisarg Ujjainkar, IIT Gandhinagar, Intern, Summer 2019
5. Kshitij Kapoor, Ashoka University, Intern, Summer 2019
6. Deepraj Pandey, Ashoka University, Intern, Summer 2019
7. Varun Gohil, IIT Gandhinagar, Intern, Summer 2018
8. Nisarg Parikh, LD College of Engineering, Summer 2018
9. Sanjith Athlur, PES University, Intern, Summer 2017
10. Indraneel Sarkar, NIT Durgapur, Intern, Summer 2017
11. Qiumin Xu, University of Southern California, Intern, Summer 2016
12. Narges Shahidi, Pennsylvania State University, Intern, Spring 2016
13. Nabarun Nag, University of Wisconsin - Madison, Intern, Summer 2015
14. Zhengyu Yang, Northeastern University, Intern, Summer 2015
15. Kevin Chang, Carnegie Mellon University, Intern, Summer 2014

Other Academic Experience

1. Graduate Research Assistant, University of Utah (June 2006 June 2011)
2. Graduate Research Intern, AMD (May 2009 September 2009)
3. Graduate Teaching Assistant, University of Utah (August 2005 May 2006)

Invited Talks

1. Computer Architecture, In-service course for Post-Graduate trained (PGT) teachers of Kendriya Vidyalaya, IIT Gandhinagar (Virtual), December 2020 (Outreach)
2. NVMs in the Memory Hierarchy: From Smartphones to Servers, IEEE Data & Storage Summit, Bangalore, November 2020.
3. How Computers Work, In-service course for Post-Graduate trained (PGT) teachers of Kendriya Vidyalaya, IIT Gandhinagar (Virtual), July 2020 (Outreach)
4. Main Memory Design Considerations for Handheld Devices: A Case for Non Volatile Memories, IIIT Delhi, February 2020.
5. Invited Panelist on *Security in Microprocessors: The Road Ahead*, MAST 2019
6. Non Volatile Main Memory for Handheld Devices: An idea whose time has come, Department of Computer Science, Ashoka University, September 2019
7. Non Volatile Main Memory for Handheld Devices: An idea whose time has come, SNIA-SDC, Bangalore, May 2019
8. Memory Architectures for Handheld Devices, ARM Bangalore, February 2019
9. Handheld Device Architectures: Are We Doing Enough? Workshop on Computer Systems, Ashoka University, Sonepat, December 2018.
10. NVMs : A Study in Use Cases, Workshop on Memory and Storage Systems, IIT Gandhinagar, Gandhinagar, December 2017.
11. Architecting Memory and Storage Hierarchies for Modern Computer Systems, Ashoka University, Sonipat, October 2017.
12. Architecting Memory and Storage Hierarchies for Future Servers, Intel Research, Bangalore, January 2017.
13. Importance of Data Locality in Servers (aka - how do I get to my data faster?), Indian Institute of Technology (IIT), Gandhinagar, November 2015
14. Importance of Data Locality in Servers (aka - how do I get to my data faster?), Indian Institute of Technology (IIT), Bombay, November 2015
15. Unlocking System Performance with NVMe Flash, Texas A & M University, September 2015
16. Unlocking System Performance with NVMe Flash, University of Texas, Austin, September 2015
17. Memory and Storage System Design for Datacenters : Challenges and Opportunities, Indraprastha Institute of Information Technology (IIIT), Delhi, April 2015
18. Memory and Storage System Design for Datacenters : Challenges and Opportunities, Indian Institute of Technology (IIT), Delhi, April 2015
19. System Level Characterization for Datacenter Applications, ICPE 2015.
20. Micron Friday Forum company-wide talk on research activities in Architecture Development Group (ADG), November 2012
21. Efficient Scrub Mechanisms for Error-Prone Emerging Memories, HPCA 2012

22. Managing Data Locality in Future Memory Hierarchies Using a Hardware Software Codesign Approach, Micron 2011
23. Managing Data Locality in Future Memory Hierarchies Using a Hardware Software Codesign Approach, Intel 2011
24. Managing Data Locality in Future Memory Hierarchies Using a Hardware Software Codesign Approach, Fusion-IO, 2011
25. Dynamic Page Placement to Manage Capacity, Replication, and Sharing within Large Caches, HPCA 2009
26. Exploring the Design Space for 3D Clustered Architectures, IBM P=ac2, 2006

Professional Service

1. Technical Program Committee Member, The 34th International Conference on VLSI Design and 19th International Conference on Embedded Systems (VLSID), January 2021
2. Technical Program Committee Member, IEEE International Conference on High Performance Computing, Data and Analytics (HiPC), December 2020
3. Technical Program Committee Member, 24^{th} International Conference on VLSI Design and Test, July 2020
4. Publicity Co-Chair, International Conference on Big Data Analytics (BDA), December 2020.
5. Invited Reviewer, IEEE Embedded Systems Letters, June 2020.
6. Invited Reviewer, Journal of Parallel and Distributed Computing (JPDC), June 2020.
7. Technical Program Committee Member, 14^{th} ACM Inter-Research Institute Student Seminar in Computer Science (IRISS), February, 2020.
8. Technical Program Committee Member, Memory Design Track Co-Chair, International Conference on VLSI Design (VLSID), January 2020.
9. Invited Reviewer, Journal of Distributed and Parallel Databases (DAPD), October 2019.
10. Invited Reviewer, Computer Architecture Letters (CAL), July, September 2019.
11. Invited Reviewer, ACM/EDAC/IEEE 56^{th} Design Automation Conference (DAC), June 2019
12. External Review Committee member, HPCA, February 2019
13. Technical Program Committee member, Big Data Analytics (BDA), December 2018
14. Technical Program Committee member, VLSID 2019
15. Technical Program Committee member, Workshop on Software Challenges to Exascale Computing, SCEC 2018
16. Invited reviewer for Journal of Parallel and Distributed Computing 2018, Microprocessors and Microsystems, 2018
17. Invited External Thesis Reviewer, IIT Delhi, Department of Computer Science and Engineering, 2018
18. Invited Reviewer, ACM/EDAC/IEEE 55^{th} Design Automation Conference (DAC), 2018
19. Program Committee Member, International Conference on VLSI Design (VLSID) 2018
20. Invited Reviewer, Integration, the VLSI Journal, Elsevier, 2017

21. Proceedings of the (Indian) National Academy of Sciences, Physical Sciences (NASA), 2017
22. National Science Foundation (NSF) CSR Panel, 2015
23. IEEE Micro Special Issue on Near Data Computation, 2015
24. ACM Transactions on Architecture and Code Optimization (ACM TACO) 2014
25. Micron internal reviewer for SRC FCRP proposals, 2012
26. IEEE/ACM International Symposium on Microarchitecture (MICRO) 2011
27. ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming 2010
28. ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming 2009
29. IEEE International Conference on Computer Architecture (HPCA) 2008
30. IEEE International Conference on High Performance Computing (HiPC), 2008

Institutional Service

1. PhD Coordinator, Department of Computer Science, Ashoka University, Spring 2020 - date
2. Member, University Committee on Innovations in Online Teaching, 2020
3. Member, University Examination Committee, 2019 - date
4. Member, Foundation Course Steering Committee, 2019 - date
5. Member, University Committee for Outreach of Science Departments (unofficial), 2019