# Handling Resistance Drift in Phase Change Memory - Device, Circuit, Architecture, and System Solutions

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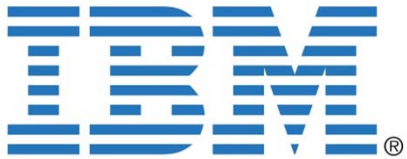

# Quick Summary

- Multi level cells in PCM appear imminent
- A number of proposals exist to handle hard errors and lifetime issues of PCM devices
- Resistance Drift is a lesser explored phenomenon
  - Will become increasingly significant as number of levels/cell increases – primary cause of "soft errors"
  - Naïve techniques based on DRAM-like refresh will be extremely costly for both latency and energy
  - Need to explore holistic solutions to counter drift

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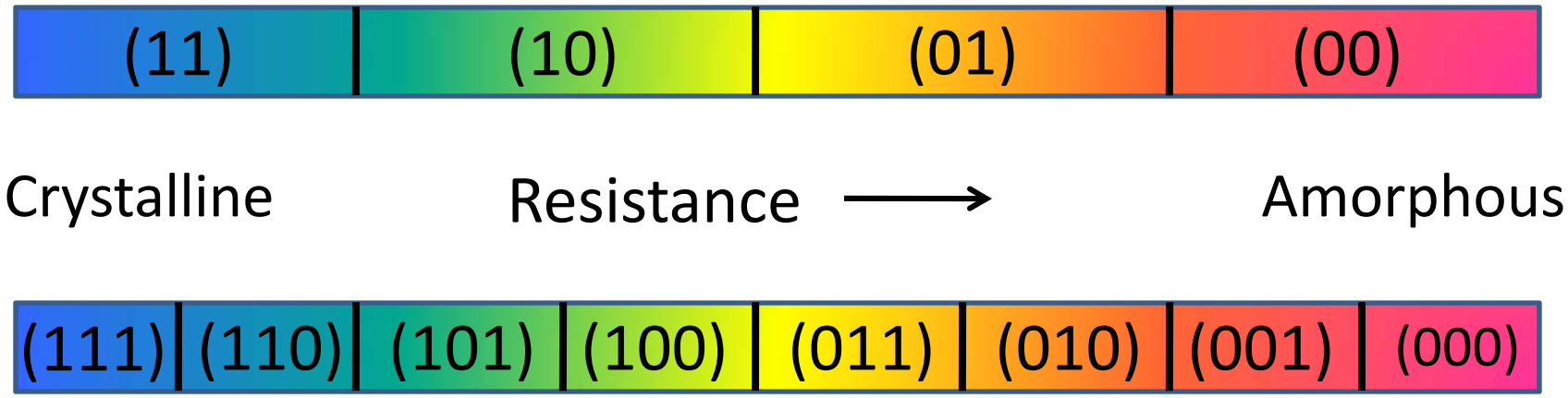
# Phase Change Memory - MLC

- Chalcogenide material can exist in crystalline or amorphous states
- The material can also be programmed into intermediate states
  - Leads to many intermediate states, paving way for **Multi Level Cells** (MLCs)

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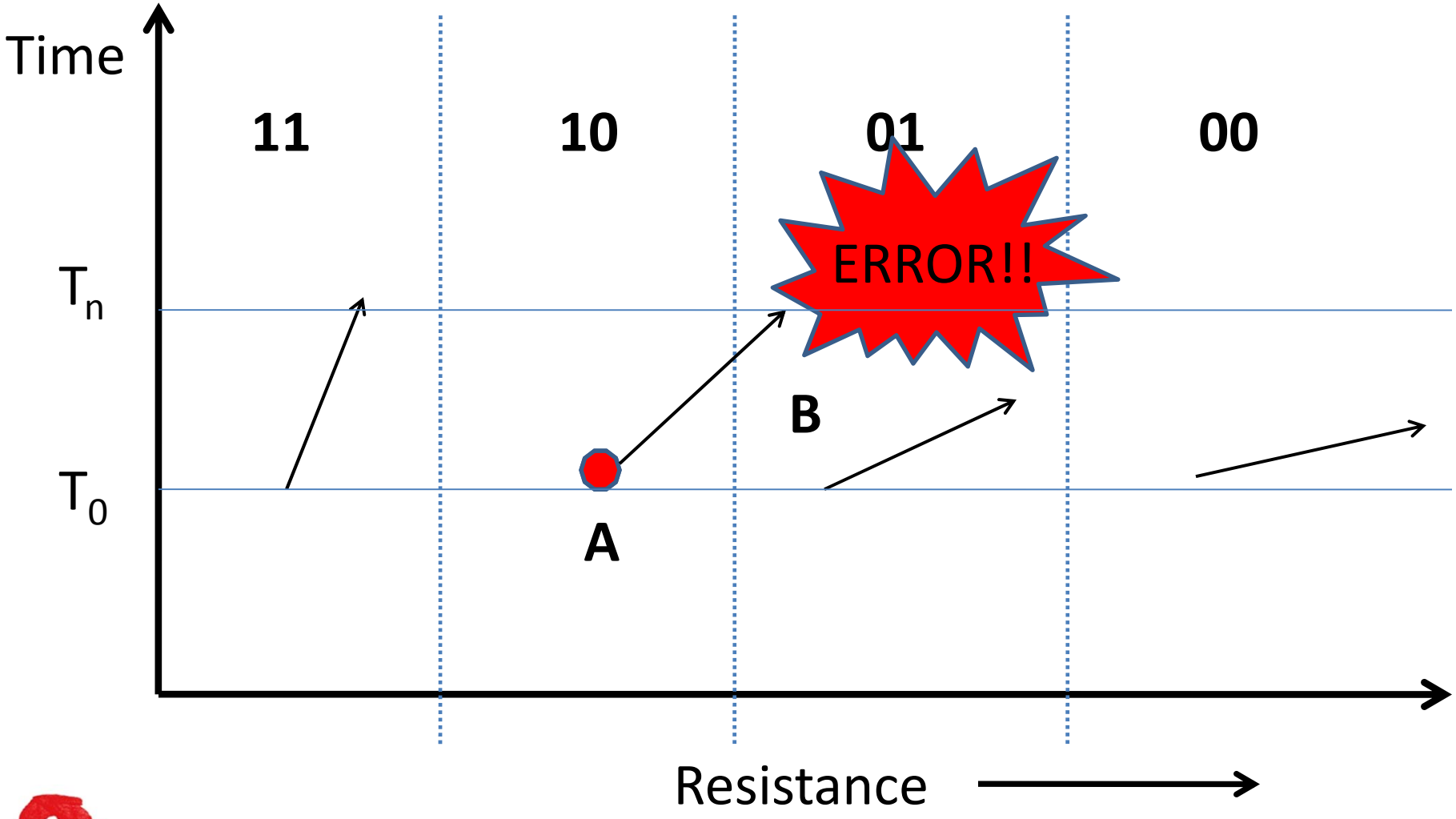
# What is Resistance Drift?

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# Resistance Drift - Issues

- Programmed resistance drifts according to power law equation -

$$R_{drift}(t) = R_0 \times (t)^{\alpha}$$

- $R_0$, $\alpha$ usually follow a Gaussian distribution
- Time to drift (error) depends on
  - Programmed resistance ($R_0$), and
  - Drift Coefficient ($\alpha$)
  - Is highly unpredictable!!

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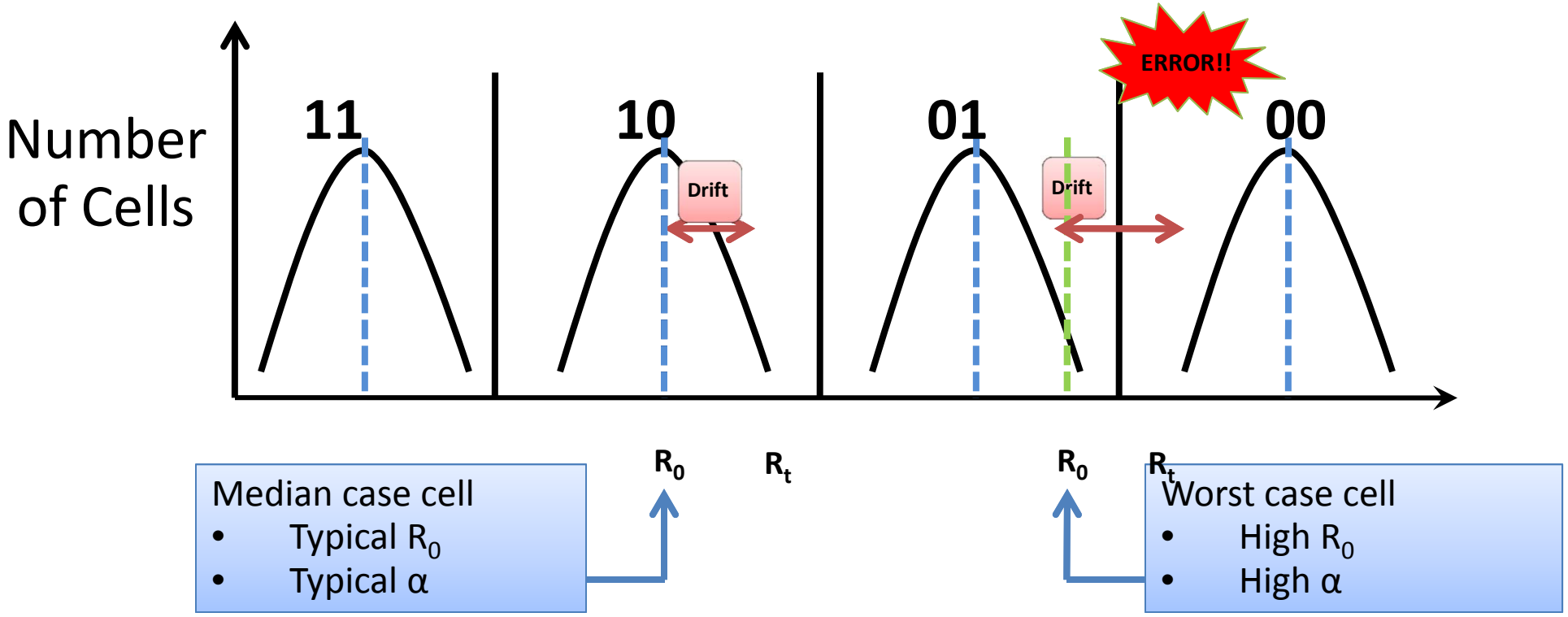
# Resistance Drift - How it happens




Scrub rate will be dictated by the
**Worst Case $R_0$ and Worst Case α**

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# Resistance Drift Data

| Cell Type | Drift Time at Room temperature (secs) |
|---|---|
| Median 11 cell | $10^{499}$ |
| Worst 11 Case cell | $10^{15}$ |
| Median 10 cell | $10^{24}$ |
| **Worst Case 10 cell** | **5.94** |
| Median 01 cell | $10^{8}$ |
| **Worst Case 01 cell** | **1.81** |


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# Naïve Solution

- Drift resets with every cell reprogram (write)
- Leverage existing error correction mechanisms e.g. ECC - has its own drawbacks
- A Full Refresh (read-compare-write) is extremely costly in PCM
  - Each PCM write takes 100 - 1000ns
  - Writing to a 2-bit cell may consume as much as 1.6nJ
  - Requires 600 refreshes in parallel

**Refresh should be reactionary NOT precautionary!**

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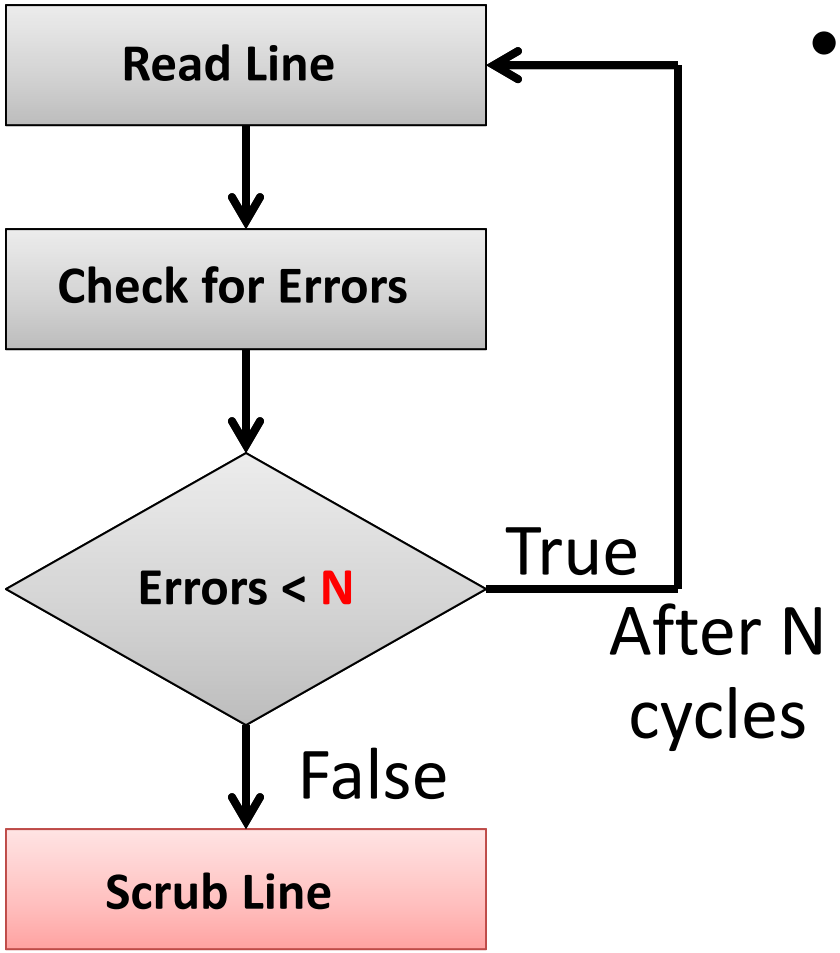
# Architectural Solutions - LARDD




- **L**ight **A**rray **R**eads for **D**rift **D**etection
  - Support for **N** Error-correcting, **N+1** error detecting codes assumed
  - Lines are read periodically and checked for correctness
  - Only after the number of errors reaches a threshold, scrubbing is performed

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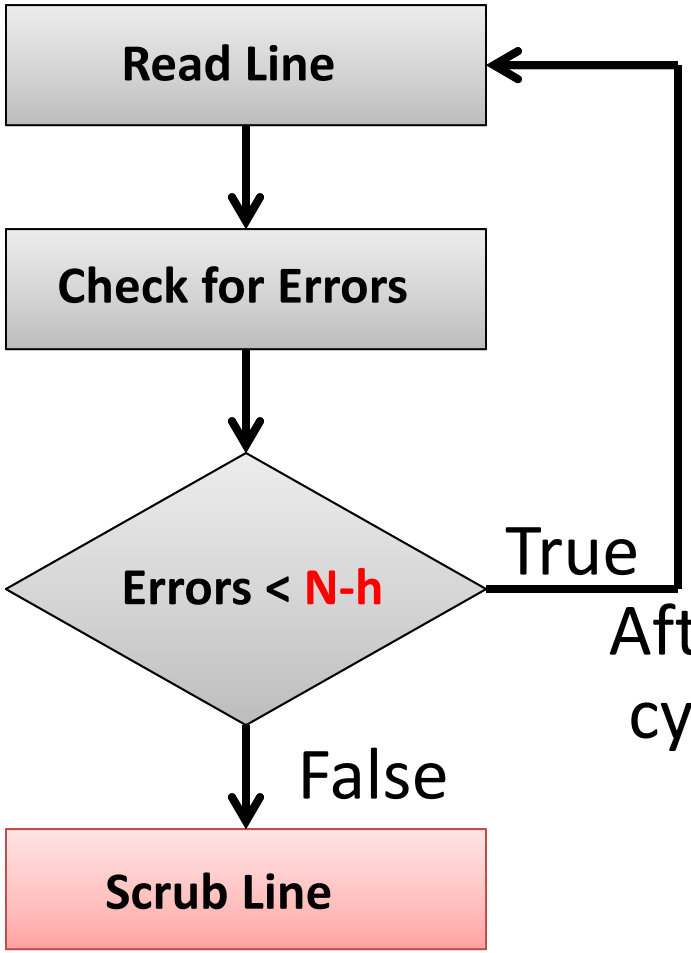
# Architectural Solutions - Headroom




- **Headroom-h** scheme – scrub is triggered if **N-h** errors are detected
  - † Decreases probability of errors slipping through
  - – Increases frequency of full scrub and hence decreases life time
- Presents trade-off between **Hard** *a*nd **Soft** *e*rrors

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# Solutions Summary

**Architectural**

- Headroom schemes
  - Trade off between error rates and lifetime

**Device**

- Precise writes
- Guardbanding

**Circuit**

- Parity based technique
  - Makes common case faster
  - Reduces overheads

**System**

- Varying scrub rates
  - Accounts for changes in operating conditions
    - Temperature
    - Hard errors

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# System Level Solutions

- Dynamic events can affect reliability
  - Temperature increases can increase α and decrease drift time
  - Cell lifetime/wearout is also an issue
  - Soft error rate depends on prevalence of drift prone states
- These effects should be taken into account to dynamically adjust LARDD frequency
- Start with a low LARDD rate
  - Double rate when errors exceed pre-set threshold
  - Mark line as defunct when hard errors exceed pre-set threshold

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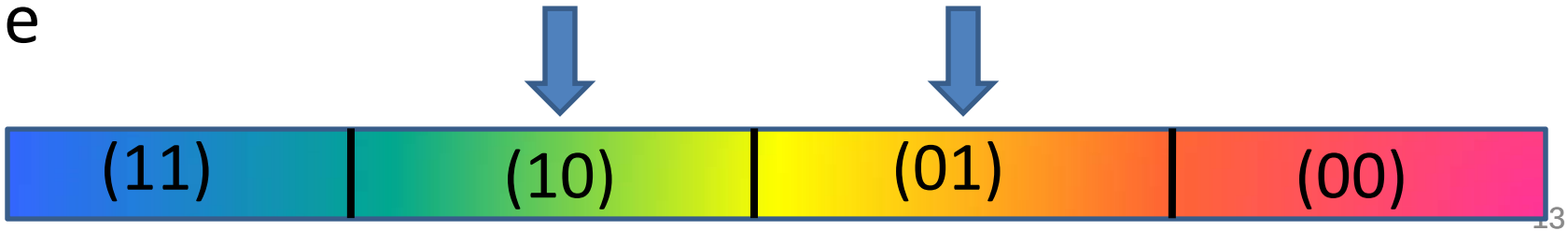
# Reducing Overheads with Circuit Level Solution

- Invoking ECC on every LARDD increases energy consumption
- ***Parity*** – like error detection circuit is used to signal the need for a full fledged ECC error detect
  - Number of **Drift Prone States** in each line are counted when the line is written into memory
  - **0** is stored as a ***Flag*** for even number of **Drift Prone States** , **1** for odd
  - The ***Flag*** is computed at each LARDD
  - A ***Flag*** mismatch invokes a full-fledged ECC
- Reduces need for ECC read-compare at every LARDD cycle

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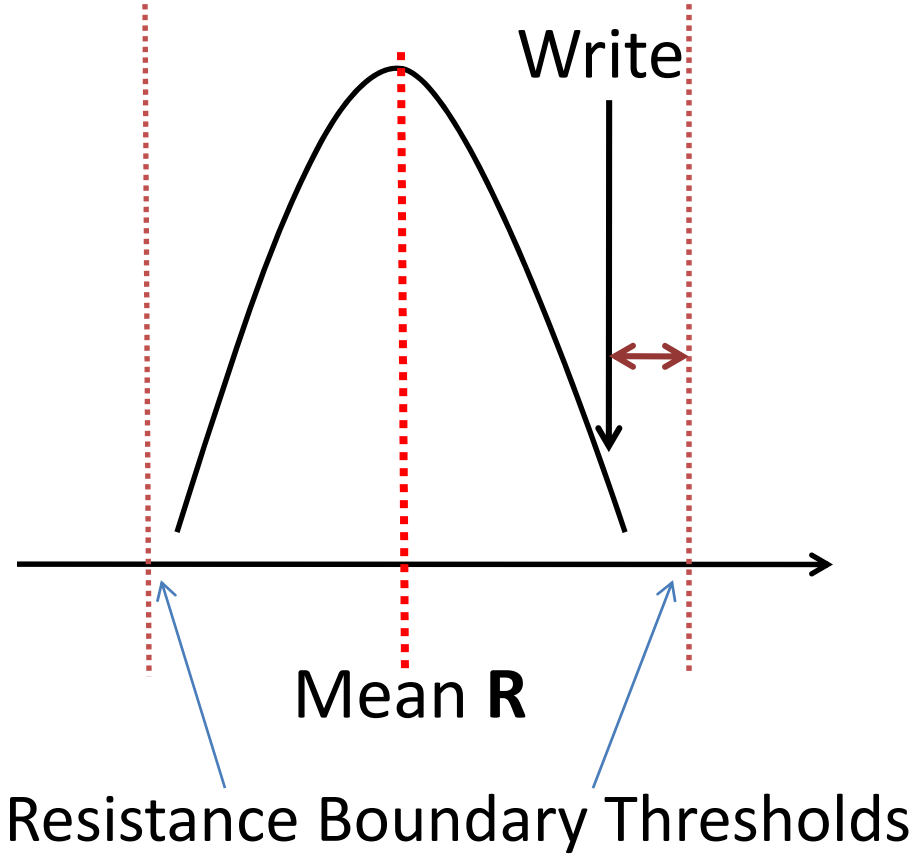
# Device Level Solution – Precise Write

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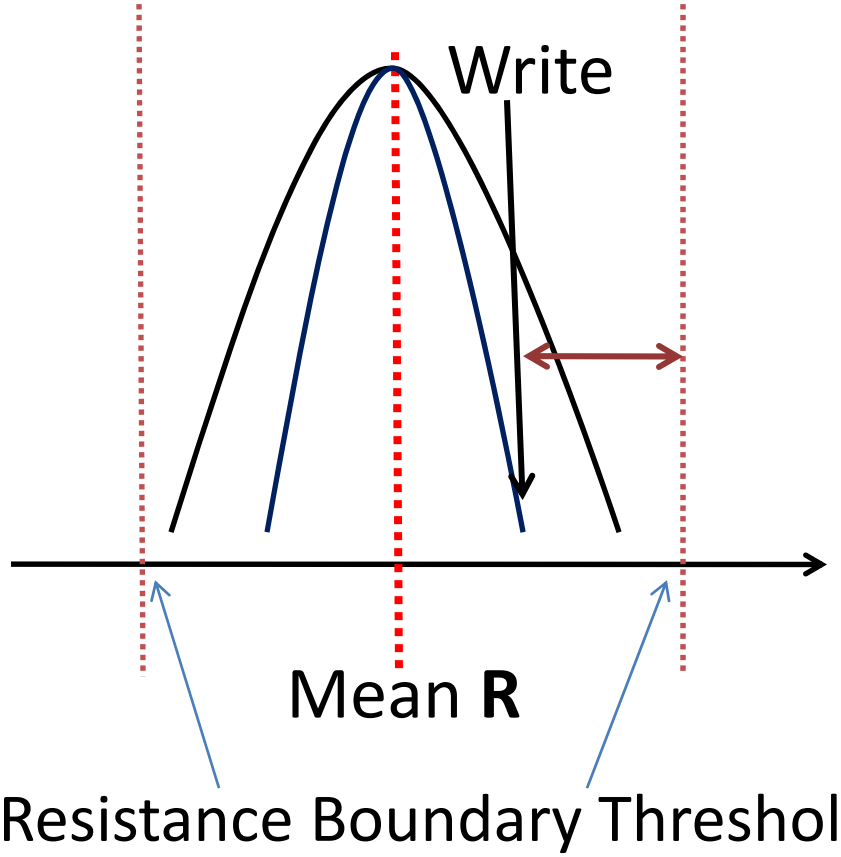
# Device Level Solution – Precise Write




Precise Writes help alleviate drift at device level but takes longer and hurts lifetime!

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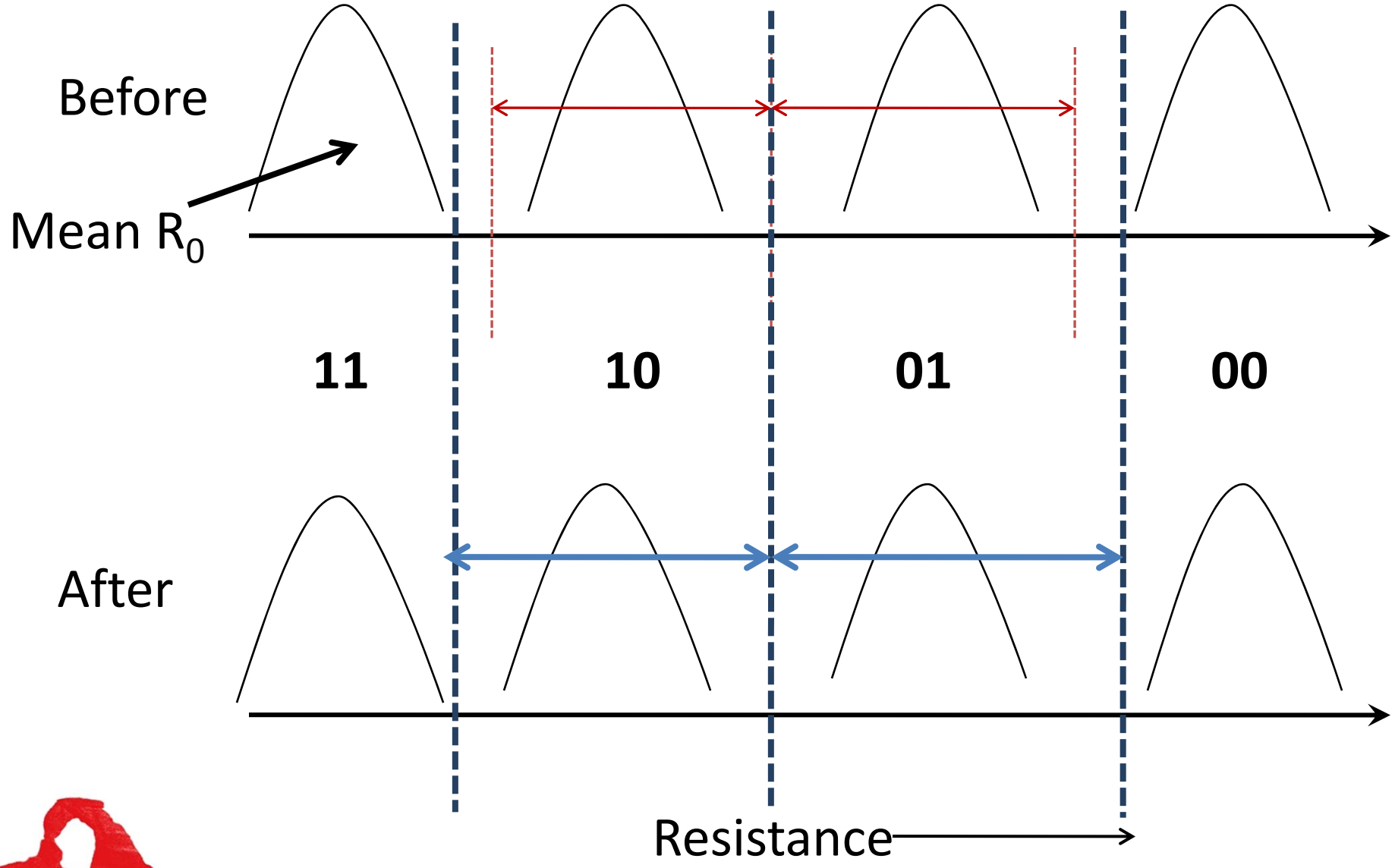
# Device Level Solution – Non Uniform Banding

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# Solutions Summary

**Architectural**

- Hetero[illegible]geneities

Error rates vs lifetime

lifetime

**Device**

- G[illegible]

Error rates vs write energy

- [illegible] between error rate write energy

**Circuit**

- Parity has [illegible]ique

Reduces ECC overheads

- Red[illegible]overheads

**System**

- Vary[illegible]es

Accounts for varying conditions

[illegible]itions

[illegible]era[illegible]e

- Han[illegible] errors

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# Conclusions

- Resistance drift will exacerbate with MLC scaling
- Naïve solutions based on ECC support are costly for PCM
  - Increased write energy, decreased lifetimes
- Holistic solutions need to be explored to counter drift at device, architectural and system levels
  - 39% reduction in energy, 4x less errors, 102x increase in lifetime
  - Work in progress!!

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Thanks!!

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